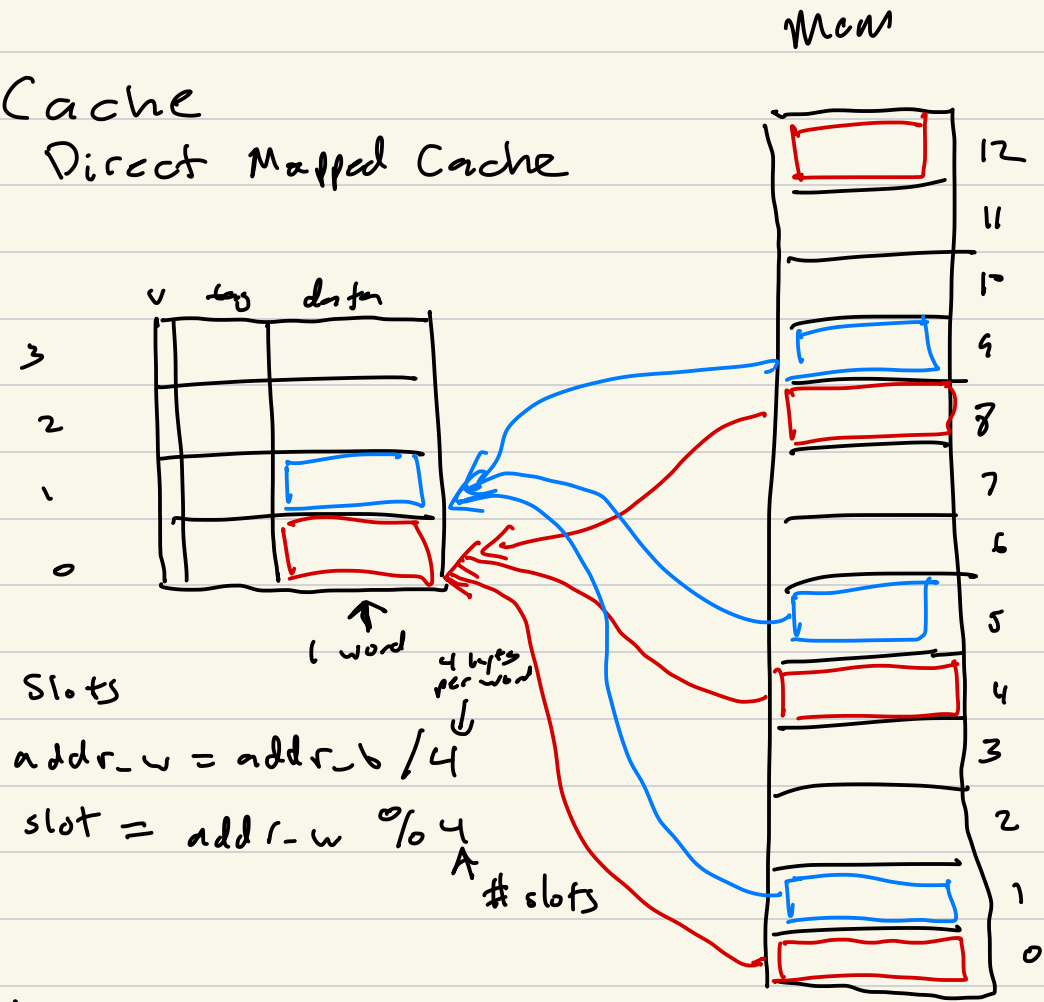
CS 315-02 Project 04 Midterm

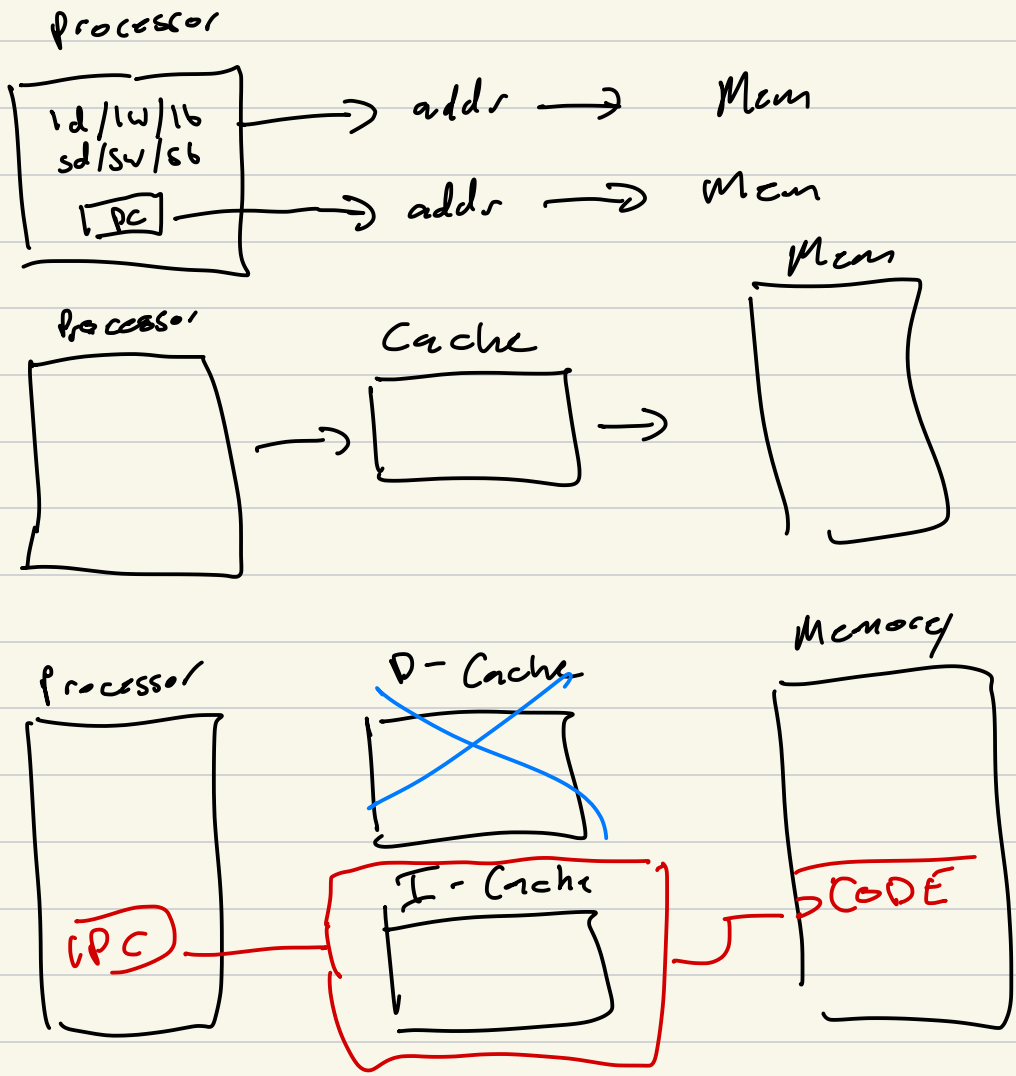
Midterm on Thursday Oct 10.

Cache

Direct Mapped Cache



Instruction Cache vs Data Cache



sw to, 8(sp)

Store mem[base.addr + offset] = rs1

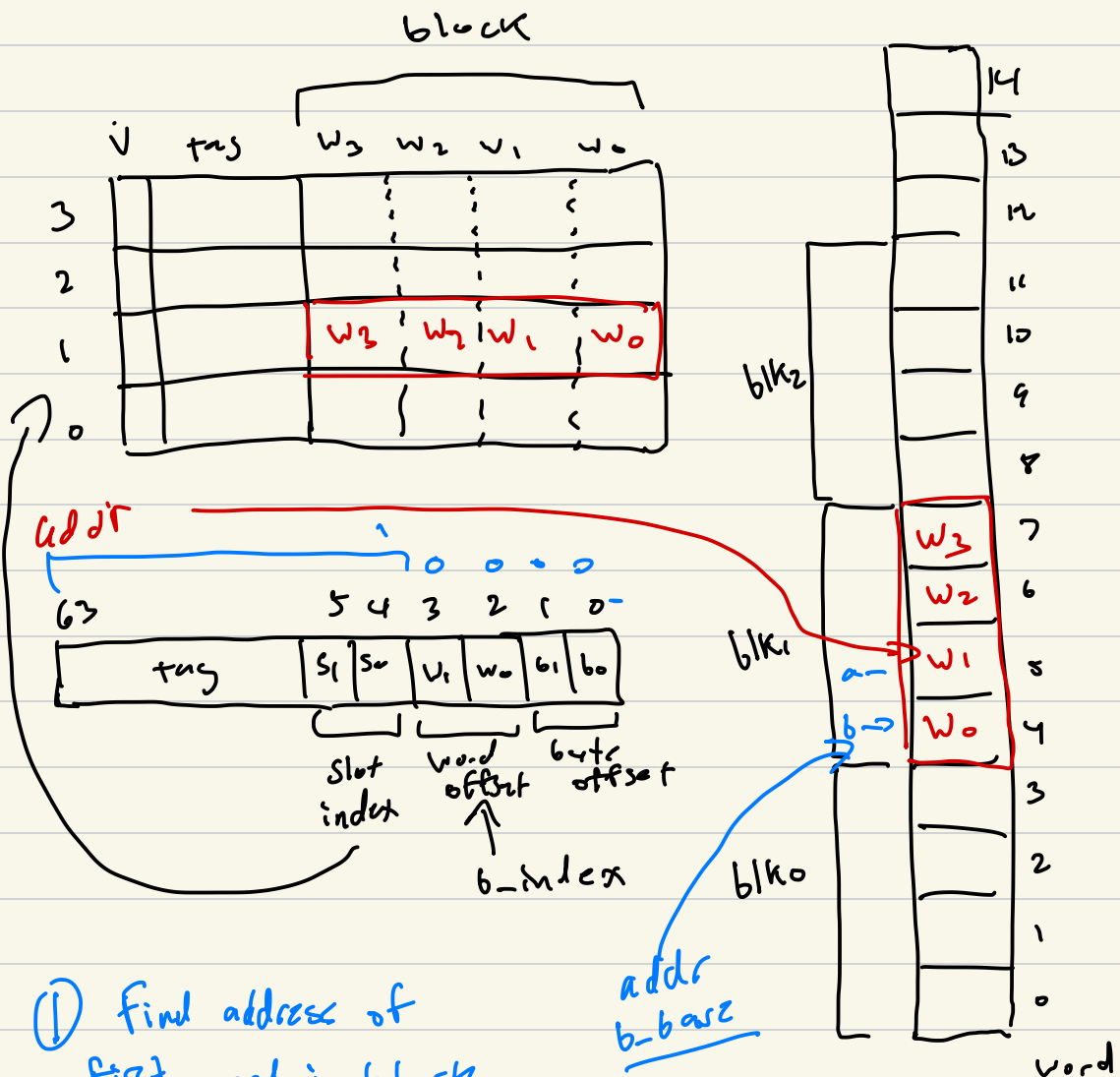
TA = rsp->regs[rs1] + imm

uint32_t *addr = (uint32_t*) TA

*addr = rsp->regs[rs2]

Block Size

Why? Principles of locality
spatial temporal



(1) find address of first word in block (in memory)

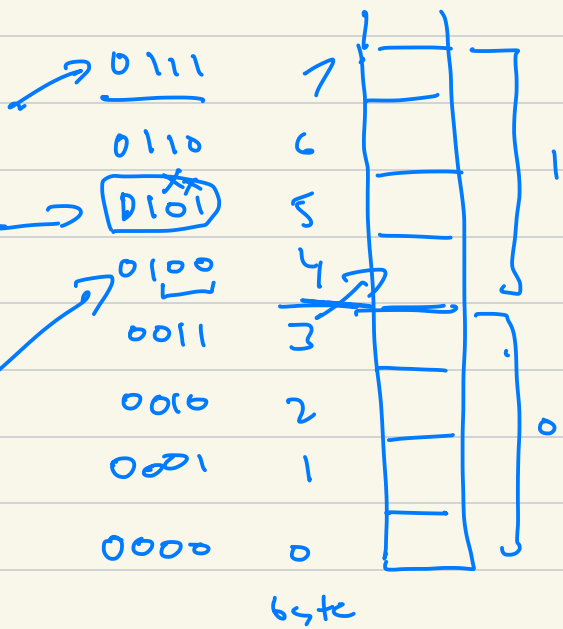
mask of lower 4 bits to 0

0 => gives base addr

14	1 0 0	0 0
&	1 0 0 0	
4	0 1 0 0	
0	0 0 0 0	

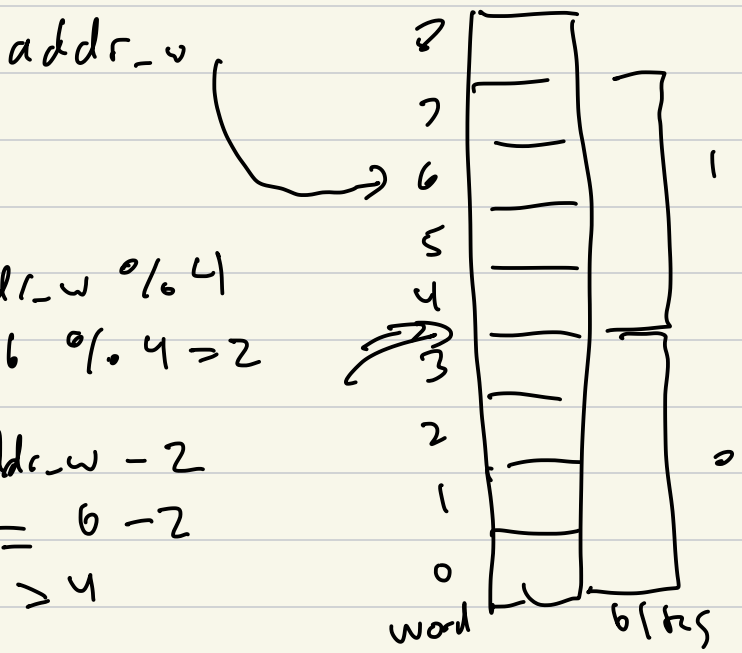
byt

7 0111



load(addr)

addr_w = addr / 4



Set Associative Cache